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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/565,145	01/19/2006	Marcel Van De Gevel	NL030871	7972

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EXAMINER	
JOHNSON, RYAN	

ART UNIT	PAPER NUMBER
2817	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/565,145	VAN DE GEVEL ET AL.	
	Examiner	Art Unit	
	Ryan J. Johnson	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. . 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-10 and 12-15* is/are rejected.

7)☒ Claim(s) *7 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/19/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. An incorrect patent number was listed on the IDS submitted January 19th, 2006 (see line 3). The IDS has been corrected with the correct patent number.

Specification

3. The disclosure is objected to because of the following informalities: Headings are absent for each section of the disclosure, hindering the readability of the application.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5,8,13 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Gay et al. (U.S. Patent No. 4,571,558 as cited by applicant).

6. Claim 1: Gay et al. discloses a crystal oscillator for generating an oscillator signal having a predetermined frequency (Figs.1,3), said crystal oscillator comprising:

a) a crystal (20) for determining said predetermined frequency;

b) a frequency-dependent negative resistance circuit connected to said crystal and having a negative resistance inversely proportional to frequency squared (amplifier 1,2 and integrators 17,10 and 16,22,14,12 function as a frequency-dependent negative resistance circuit. Fig.1 and the abstract describe an amplifier followed by two integrators in series. The output current of the first integrator will be proportional to the time integral of the current coming from the amplifier. The output of the second integrator is proportional to the double time integral of the current from the amplifier. It is well known in the art that a circuit that utilizes two integrators and an amplifier in series in a crystal oscillator as disclosed by Gay et al. will result in a negative resistance inversely proportional to the frequency squared.)

c) means for controlling the amplitude of said oscillator signal, either by a clipping mechanism inside the frequency-dependent negative resistance circuit, or by an amplitude control loop controlling the value of the frequency-dependent negative resistance (the amplifier comprising transistors 1,2 and current sources 7 and 3 is a standard configuration for a long-tailed pair. The input of each differential input, the base of transistors 1 and 2, are tied together with resistor R1. Since there is no amplitude control, the amplifier is configured as a clipping amplifier and will clip between the power supplied at node 8 and ground, node 15).

7. Claim 2: Gay et al. discloses wherein said frequency-dependent negative resistance circuit comprises a first integrator circuit (16,11,12,14; col.3,19-25) having an output connected to said crystal (through resistor 18; col.3,31-39), a second integrator

circuit (17,10) having an input connected to said crystal (through transistor 1), and an amplifier circuit (1,2) for controlling the amplitude of said oscillator signal (col.2,42-58).

8. Claim 3: Gay et al. discloses wherein said output of said first integrator circuit is a low-impedance voltage output (the output of the first integrator circuit is a voltage applied to resistor 18, and is low impedance due to the voltage being applied from transistor 14; col.3,31-35), and said second integrator circuit is a low-impedance current input (current is input from current source 7 to the integrator comprising capacitor 17).

9. Claims 4,5: Gay et al. discloses wherein said amplifier circuit is a clipping amplifier circuit or a gain-controlled amplifier circuit and comprises a transconductance amplifier (transistors 1 and 2 comprises a standard configuration of a long-tailed pair differential amplifier. Therefore, the amplifier is configured as a clipping amplifier and will clip between the power supplied at node 8 and ground, node 15. The amplifier also comprises a transconductance amplifier since the output current seen at node 9 is in response to the input voltage seen at node 6; Fig.1).

10. Claim 8: Gay et al. discloses wherein said amplifier circuit comprises a differential pair of transistor means (transistors 1,2; Figs.1,3).

11. Claim 13: Gay et al. discloses wherein said crystal oscillator (20) has a single-pin configuration, where one terminal of said crystal is connected to a reference potential (ground; Figs.1,3).

12. Claim 15: Gay et al. discloses a latch-out circuit (63) for preventing an undesirable stable bias point of said amplifier circuit (transistor 63 is provided to inhibit

transistor 55 from becoming saturated, thereby preventing an undesirable condition in the current source 3. col.7,41-51).

13. Claims 1 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Perkins (U.S. Patent No. 4,646,033 as cited by applicant).

14. Claim 1: Perkins discloses a crystal oscillator for generating an oscillator signal having a predetermined frequency (Fig.1), said crystal oscillator comprising:

a) a crystal (14) for determining said predetermined frequency;

b) a frequency-dependent negative resistance circuit connected to said crystal and having a negative resistance inversely proportional to frequency squared (amplifier 22 and integrators 40,38 and 56,58 function as a frequency-dependent negative resistance circuit. Fig.1 and the abstract describe an amplifier followed by two integrators in series. The output current of the first integrator will be proportional to the time integral of the current coming from the amplifier. The output of the second integrator is proportional to the double time integral of the current from the amplifier. It is well known in the art that a circuit that utilizes two integrators and an amplifier in series in a crystal oscillator as disclosed by Perkins will result in a negative resistance inversely proportional to the frequency squared.); and

c) means for controlling the amplitude of said oscillator signal, either by a clipping mechanism inside the frequency-dependent negative resistance circuit, or by an amplitude control loop controlling the value of the frequency-dependent negative resistance (the amplifier 22 and current source 34 is a standard configuration for a long-

tailed pair. The input of each differential input, the base of transistors 24 and 26, are tied together with resistor 36. Since there is no amplitude control, the amplifier is configured as a clipping amplifier and will clip between the power supplied at VCC and ground).

15. Claim 6: Perkins discloses a direct current feedback loop for biasing said first and second integrator circuits (transistors 58 and 40 are biased by negative DC feedback; col.3,25-41).

16. Claims 1 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Dent et al. (U.S. Patent No. 6,768,389).

17. Claim 1: Dent et al. discloses a crystal oscillator for generating an oscillator signal having a predetermined frequency (Fig.5B), said crystal oscillator comprising:

a) a crystal (14) for determining said predetermined frequency;

b) a frequency-dependent negative resistance circuit connected to said crystal and having a negative resistance inversely proportional to frequency squared (amplifier 46 and integrators 40,42 and 48,50 function as a frequency-dependent negative resistance circuit. Fig.5B shows an amplifier shows an integrator, an amplifier, and a second integrator all in series. The output current of the first integrator will be proportional to the time integral of the current coming from the crystal 14. The output of the second integrator is proportional to the double time integral of the current. It is well known in the art that a circuit that utilizes two integrators and an amplifier in series in a crystal oscillator as disclosed by Dent et al. will result in a negative resistance inversely proportional to the frequency squared.); and

c) means for controlling the amplitude of said oscillator signal, either by a clipping mechanism inside the frequency-dependent negative resistance circuit, or by an amplitude control loop controlling the value of the frequency-dependent negative resistance (Dent et al. describes 46 as a limiter, a type of clipping amplifier; col.6,6-28)

18. Claim 14: Dent et al. discloses wherein said crystal oscillator has a two-pin configuration (one pin of the crystal is connected to the input of the circuit, while the other pin is connected to the output of the circuit. This could be considered a two-pin configuration; Fig.5B).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 9,10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dent et al. (U.S. Patent No. 6,768,389) in view of Torelli et al. (U.S. Patent No. 4,749,956).

21. Claims 9,10: Dent et al. discloses the limitations of claims 1 and 2. Dent et al. also discloses feedback capacitors (C2; Fig.5B) for each integrator. Dent does not explicitly disclose the amplifier being one-stage or two-stage. Torelli et al. discloses that an operational amplifier is capable of being either one or two stages based on design considerations (col.2,12-28). The selection of something based on its known suitability for its intended use has been held to support a prima facie case of obviousness.

Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used either a single-stage or double-stage operational amplifier, as disclosed by Torelli et al., as the operational amplifiers (40,48) as disclosed by Dent et al. in order to have provided a suitable operational amplifier which would have performed the equivalent function as operation amplifiers.

22. Claim 12: Dent discloses a resistor (49) connected in series with said feedback capacitor (C2; Fig.5B).

Allowable Subject Matter

23. Claims 7 and 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

24. The following is a statement of reasons for the indication of allowable subject matter: "said direct current feedback loop comprises a resistor connected in parallel with said crystal" in the context of claim 7 could not be found in prior art.

"wherein a first transistor element of the output stage ... is biased by a second transistor element" in the context of claim 11 could not be found in prior art.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Musa (U.S. Patent No. 3,676,801) discloses a crystal oscillator circuit without load capacitors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan J. Johnson whose telephone number is 571-270-1264. The examiner can normally be reached on Monday - Thursday, 9:00 am - 5:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RJJ/

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